Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

The invention provides five new methods for the formation of an improved liquid-crystal-on-silicon display. The device structure is enhanced by the photolithographic creation of alignment posts among the mirror pixels of the micro-display. The five methods accommodate the fabrication of an optical interference multilayer, which improves the image quality of the reflected light. The five methods of the invention provide:

- silicon dioxide posts by wet etching
- amorphous silicon posts by plasma etching
- silicon nitride posts by plug filling
- insulation material posts by lift-off, and
- polyimide posts by photosensitive etching.

Specification

The specification is objected to under 37 CFR 1.75(d)(1) and MPEP § 608.01(o) in view of subject matter of claims 8-32 not being described in the specification.

Claim 8 has been amended and is now in accordance with Figs. 4-6 of the specification. In addition, a paragraph has been added to page 9 (bottom of the page) in which the processing steps of Figs. 4-6 have been detailed. Included in this paragraph are the reference numbers that have been used in Figs. 4-6, making easy comparison between the text of the paragraph and the processing steps of Figs. 4-6 possible. The text that has been used for the paragraph that has been added to page 9 follows the processing steps that have been described in the specification for Figs. 4-6, in addition this text follows the amended claim 8.

No new matter has been added to the Application by the amendments that have been provide, the amendments provide further clarification of the specification and of the claims in addition to correcting errors in both the original specification and claim 8.

Applicant is confident that the amendment that has been provided to claim 8 removes Examiner's objection to claims 8-32 since claims 9-32 under the objection are dependent claims to amended claim 8.

In light of the foregoing response, applicant respectfully requests that the Examiner's objection to claims 8-32, under 37 CFR 1.75(d)(1) and MPEP \S 608.01(o), be withdrawn.

Claim rejections - 35 U.S.C. § 112

Reconsideration of the rejection of claims 2-5 and 22 under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is respectfully requested based on the following.

The Examiner is thanked for pointing out the various antecedent basis problems in the claims. The claims have been carefully reviewed and amended to correct those problems the Examiner pointed out, in addition to others. All claims are now believed to be in allowable condition.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 2-5 and 22 under 35 U.S.C 112, second paragraph, be withdrawn.

Claim rejections - 35 U.S.C. § 102

Reconsideration of the rejection of claims 1, 2, 5, 6, and 33 under 35 U.S.C 102(e) as being anticipated by Moore et al. (US Patent 6,051,446) is respectfully requested based on the following.

The rejection of claim 33 is considered moot since claim 33 has been cancelled.

Moore et al. provide for the formation of a thin liquid crystal transducer cell having self-aligned support pillars. A significant portion of the Moore et al. invention addresses parts of the required processing sequence that do not relate to the instant invention, since the instant invention addresses, see claims 1 and 8, the formation of insulating material alignment posts (that are associated with active device structures). In view of this, only these portions of Moore et al. that concern themselves with the formation of support pillars 305, Fig. 3CC, need to be addressed here.

To create support pillars 305, Moore et al. Figs. 3AA through 3CC and corresponding text:

- provide a layer 314, Fig. 3AA 3AC of lower interconnect
 metal
- deposit a layer 312 of upper intermetal dielectric over the surface of layer 314
- create a via through the layer 312, the via is filled with a metal (tungsten) to established a point of electrical contact on the surface of layer 312 with layer 314, and
- deposit a thick layer of silicon nitride over the surface of layer 312, patterned and etch to create support pillars 314 on the surface of layer 312 of upper intermetal dielectric.

The balance of the Moore et al. invention addresses the formation of a reflective pixel electrode that is aligned with the created support pillars.

From the above the following conclusions can be drawn:

• the support pillars 305 that are created by Moore et al. comprise silicon nitride, the support pillars that are created by the instant invention comprise silicon oxide (support pillars 71, Fig. 8) or amorphous silicon (support pillars 101, Fig. 10) or silicon nitride (support pillars 122, Fig. 13) or an insulation material (support pillars 153, Fig. 17) or polysilicon (support pillars 191, Fig. 19); since

the support pillars that are created by Moore et al. comprise and are limited to silicon nitride, the instant invention provides for the creation of support pillars of a variety of materials, using a variety of processing sequences and resulting in a variety of support pillars that can be used for and adapted to a variety of applications

- the support pillars that are created by Moore et al. comprise silicon nitride only, the support pillars of the instant invention comprise an optical interference layer in addition to an optical interference multilayer stack, as specified in amended claim 1; the methods and limitations that apply for the creation of the optical interference multilayer stack and the optical interference layer is further detailed in claims 3 through 7 of the invention
- the support pillars that are created by Moore et al. comprise silicon nitride only, the etching of a layer of silicon nitride is well known in the art; by contrast, the invention provides for, as pointed out, a variety of materials for the support pillars in further provides, for each of the material, a method of etching the material, see claims 9, 12, 13, 17, 21 and 22, 23, 24, 25, 27, 29, 32; examples that apply to the instant invention: silicon dioxide posts (created by) wet etching, amorphous silicon post (created by) plasma etching, etc.

- the instant invention creates the support posts over the surface of a layer of OIL; Moore et al. create support posts over the surface of a layer 212 of dielectric; the functionality of the liquid-crystal display that is formed using the support pillars of the invention is therefore completely different from the functioning of the liquid-crystal display that is created by Moore et al.; specifically, Moore et al. create support pillars that are adjacent to the reflexive pixel electrode 308/321, Fig. 3FC; the support pillars of the instant invention can be located in any position with respect to the pixels of the display, no symmetry of construction of the support pillars (with respect to the pixels) is required meaning that a large number of support pillars can be created over the surface of a wafer for additional support
- the support pillars of the invention are created on the surface of a Optical Interference Layer (OIL), the support pillars of Moore et al. (see Fig. are places on the surface of a layer (312, Fig. 3FC) of dielectric and are placed inside openings that have been etched through the pixel electrode 306, Fig. 3DB of Moore et al. (layers 308/310 of Fig. 3FC); this also provides for different support for the support pillars.

In addition, claim 1 has been amended. Since claims 2, 5 and 6 within this rejection are dependent upon amended claim 1 and carry all of the limitations of amended claim 1, applicant additionally asserts that those remaining claims may not also properly be rejected under 35 U.S.C 102(e) as being anticipated by Moore et al. (US Patent 6,051,446), for reasons cited by the examiner.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1, 2, 5, 6, and 33 under 35 U.S.C 102(e) as being anticipated by Moore et al. (US Patent 6,051,446), be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claims 3, 4 under 35 U.S.C 103(a) as being unpatentable over Moore et al. (US Patent 6,051,446) in view of Lee (US Patent 4,827,870) is respectfully requested based on the following.

The differences between the instant invention and the invention provided by Moore et al. have been argued supra. The instant invention provides for the creation of liquid-crystal-on-silicon displays whereby methods of photolithography are

applied, using five methods for these creations. These methods have been specified in detail using Figs. 4-6 as common processing steps, Figs. 7 and 8 for a first method, Fig. 9 and 10 for a second method, Figs. 11-13 for a third method, Figs. 14-27 for a fourth method and Figs. 18-20 for a fifth method. The claims follow a similar sequence with claim 9 (and its dependent claims) addressing a first method, claim 13 (and its dependent claims) addressing a second method, claim 17 (and its dependent claims) addressing a third method, claim 24 (and its dependent claims) addressing a fourth method, claim 29 (and its dependent claims) addressing a fifth method.

Claims 1-8 have been provided to specify the creation of an optical interference layer (claims 1, 2, 5) and an optical interference multilayer stack (claims 1, 4), alignment posts (claims 1, 6, 7) of the invention comprising optical interference layer and an optical interference multilayer stack. In order for the claims of claim set 1-8 to be complete, claims 3 and 4 must be part of this set of claims.

That Lee teaches an apparatus for applying multilayer optical interference coating on complex curved substrates may provide a method for the implementation of the instant invention but this does not negate the originality of the instant

invention. The apparatus that is provided becomes a potential tool for the implementation of the invention but does therefore not affect the instant invention in being original and therefore patentable. By not providing any of the claims of the claim set 1-8, a feature of the alignment posts of the invention would not be specified, making the set of claims incomplete.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 3, 4 under 35 U.S.C 103(a) as being unpatentable over Moore et al. (US Patent 6,051,446) in view of Lee (US Patent 4,827,870), be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claim 7 under 35 U.S.C 103(a) as being anticipated by Moore et al. (US Patent 6,051,446) in view of Sato et al. (US Patent 5,397,139) is respectfully requested based on the following.

Sato et al. (US Patent 5,379,139) specifies, col. 3, lines 24 e.a., "the thickness is reduced to less than 3 microns, e.g. 2 +- 0.5 microns, which is suitable ...". Claim 7 specifies a lower limit of 0.3 microns which is considerable lower than the lower limit that is provided by Sato et. al, indicating that the

invention allows for the creation of considerably thinner crystal devices, which provides a considerably extended limit in creating thin crystal devices.

In addition, the fact that a device or device feature is created that may or have identical or close to identical physical dimension after the device or the device feature has been completed has no bearing on the uniqueness of the process that is used for this creation. It is entirely feasible to create two elements that have identical physical dimension upon completion whereby yet the processes that are used for these creations are unique and are therefore each patentable.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claim 7 under 35 U.S.C 103(a) as being anticipated by Moore et al. (US Patent 6,051,446) in view of Sato et al. (US Patent 5,397,139) be withdrawn.

Claim rejections - 35 U.S.C. § 103

Reconsideration of the rejection of claim 33-36 under 35 U.S.C 103(a) as being unpatentable over Moore et al. (US Patent

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6,051,446) in view of Wright et al. (US Patent 5,801,800) is respectfully requested based on the following.

The rejection of claims 33-34 is considered mot since these claims have been cancelled.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

The invention provides five new methods for the formation of an proved liquid-crystal-on-silicon display. The device structure is enhanced by the photolithographic creation of alignment posts among the mirror pixels of the micro-display. The five methods accommodate the fabrication of an optical interference multilayer, which improves the image quality of the reflected light. The five methods of the invention provide:

- silicon dioxide posts by wet etching
- amorphous silicon posts by plasma etching

- silicon nitride posts by plug filling
- insulation material posts by lift-off, and
- polyimide posts by photosensitive etching.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned:

"Version with markings to show changes made."

Respectfully submitted,

Stephen B. Ackerman (Reg. No 37,761)

Version with markings to show changes made

IN THE SPECIFICATION

1) page one, first paragraph, please replace this paragraph with the following paragraph:

This <u>Application</u> is related to Patent Application Serial

No. [-----] <u>09/262,910 (CS98-077)</u> Su Yong Jie, Ravi Sankav and

Han Zhi Ciang filed [as ----- (CS 98-077)] <u>on 03/05/99</u> and

to Serial No. [-----] <u>09/259,778 (CS98-078)</u> by Sudipto R. Roy

filed [as ---- (CS 98-078)] <u>on 03/01/99</u>, all of Chartered

Semiconductor Manufacturing LTD of Singapore Technologies.

2) page 1, second paragraph, replace the paragraph with the following paragraph:

The picture quality of liquid crystal displays [from the simple] that are created using as simple a design as seven segments to complex designs using millions of pixels is determined by the structure that is used to control the variation of the [thickness] height of the pixels and the [position] location of the external wires after wafer processing has been completed. There are known processes for creating

insulating alignment posts based on preformed glass microspheres and rods; relatively low series resistance posts can be obtained by means of selective deposition of polysilicon and metallic silicide.

3) page 5, second and third paragraphs, replace these two paragraphs with the following paragraph:

Figs. 1 through 3 schematically illustrate in cross-sectional representation (Fig. 1) and top view (Figs. 2 and 3) a preferred embodiment of the device structure of the present invention.

Figs. 4 through 6 show the processing steps that are commonly shared between all five methods of the invention. The base silicon substrate with the formed metallic pixels on the display device is shown in Fig. 4.

[The process flow for making the alignment posts and the optical interference layers by the five process categories is shown in Figs. 5 to 19.]

4) page 5, fifth paragraph, replace this paragraph with the following paragraph:

Fig. 6 shows the optical interface [layers] <u>layer</u> deposition.

- 5) page 5, sixth paragraph, replace this paragraph with the following paragraph:
- Fig. 7 shows the deposition of [the] a thick layer of silicon oxide [on top of the OIL] over the surface of the Optical Interface Layer (OIL).
- 6) page 5, seventh paragraph, replace this paragraph with the following paragraph:
- Fig. 8 shows the photomask after [etch off of the] excess silicon oxide has been removed from the surface of the OIL [with] by applying wet etch processing.
- 7) page 5, after the fifth paragraph, add the paragraph:
- Figs. 7 and 8 show the first method of the invention, that is the method that applies wet etch processing, as follows:

8) page 6, before the first paragraph, add the following paragraph:

Figs. 9 and 10 show the second method of the invention, that is the method that applies amorphous silicon plasma etching, as follows:

9) page 6, before the third paragraph, add the following paragraph:

Figs. 11 through 13 show the third method of the invention, that is the method that provides nitride plug filling, as follows:

10) page 6, before the sixth paragraph, add the following paragraph:

Figs. 14 through 17 show the fourth method of the invention, that is the method that applies insulating material lift-off, as follows:

11) page 7, before the second paragraph, add the following paragraph:

Figs. 18 and 19 show the fifth method of the invention, that is the method that makes us of photosensitive polyimides, as follows:

- 12) page 6, replace the third paragraph with the paragraph:
- Fig. 11 shows the <u>deposition of a thick [oxide] layer of oxide</u> [of top of] <u>over the surface of the OIL as a first step in forming [the] plasma plugs of silicon nitride.</u>
- 13) page 6, fifth paragraph, replace this paragraph with the following paragraph:
- Fig. 13 shows the result of silicon nitride etch-back [with] and plasma [and] oxide removal [with] by applying wet etching.
- 14) page 6, sixth paragraph, replace this paragraph with the following paragraph:
- Fig. 14 shows the results of the <u>successive</u> deposition [consequence] of a thick <u>layer of photoresist</u>, [SiO] <u>a layer of silicon oxide (SiO) deposited</u> by thermal evaporation[,] and a thin [resist] layer <u>of [resist] photoresist over the surface of the successive deposition successive deposition [successive deposition successive deposition [successive deposition successive deposition successive deposition successive deposition [successive deposition successive deposition deposition deposition deposition successive deposition deposit</u>

the OIL, this [prior to the deposition of] in preparation for the creation of the insulation material posts.

15) page 7, second paragraph, replace this paragraph with the following paragraph:

Fig. 18 shows [the] <u>a cross-section after [the] a layer of</u> photosensitive polyimide [is] <u>has been deposited over the</u> surface of the OIL.

16) page 7, third paragraph, replace this paragraph with the following paragraph:

Fig. 19 shows [the] \underline{a} cross-section after [the post] photomasking and development of the photosensitive polyimide \underline{for} formation of alignment posts.

17) page 7, fourth paragraph, replace this paragraph with the following paragraph:

Fig. 20 [schematically illustrates in cross-sectional representation] shows a cross section of one [type of final] embodiment of [this] the present invention [for this liquid-crystal-silicon display device].

18) page 9, the first two paragraphs, replace these paragraphs with the following two paragraphs:

The [process] <u>processing</u> steps for making the alignment posts and optical interference layers by means of the various [photolithographic categories is] <u>methods of the invention are</u> shown in [Figures] <u>Figs. 4</u> to 20.

Starting with Fig. 4, there is shown the cross section of a substrate 9 on the surface of which a sequence of layers of semiconductor materials is deposited, as follows: the conductive metallic (or poly) layer 30 is formed over the layer 40 of silicon oxide [40], which is formed [on top] over the surface of [the second] a first metal layer [20] 41, Fig. 5, [on the IC]. Prior to formation of the layer 40 of silicon oxide [40], the metal [20 as] bond pad 20, Fig. 5, is [deposited] created on the surface of layer 41 of [silicon dioxide 41] first level metal.

[A] The silicon semiconductor substrate [09] 9 is coated with an insulating layer 16 of silicon dioxide [insulating layer 15] and has active devices [therein] in layer 15 in or on the surface of substrate 9. [and an metal layer (metal 1) 16 upon which silicon dioxide 41 is formed]. Then a photoresist layer (not shown) is formed over the layer 30 of second metal [30] to [construct]

pattern and etch [the] pixels 30. The photoresist (not shown) is exposed and a portion removed [to provide] such that each pixel 30 retains a metallic layer, which [shall act] acts as a mirror reflector for [the] light incident upon [said] pixel 30.

19) page 11, last paragraph, replace this paragraph with the following paragraph:

A silicon oxide layer 110, about 1 micron thick, is deposited on top of the OIL 60, as shown in Fig. 11. The photomask is formed over the oxide, except the location of each alignment post, and a plasma oxide etching is used to remove the silicon oxide not covered by the photomask, creating cavities 120, including some or all of the OIL at the base of the post cavity. Subsequently the post cavities 120 are filled with silicon nitride 121 deposited by plasma enhanced chemical vapor deposition (PECVD). [[]The plasma enhancement provides low temperature deposition [(] of about 200 degrees centigrade [)] lower than conventional PECVD [during the] deposition of a layer of silicon nitride [over that obtained without the existence of the plasma]. Without the plasma, the nitride deposition is in the range of 700 degrees centigrade []].

20) page 9, after the last paragraph, please add the paragraph:

The processing steps that are presented in Figs. 4 through 6 can be summarized as follows;

- the process starts with a silicon semiconductor wafer 9 having a pattern 15 of active device structures therein and thereon
- (optionally) a layer 16 of insulation material is formed over the surface of wafer 9
- a first metallic layer 41 is formed over the surface of the layer 16 of insulating material
- a second metallic layer 20 is formed over the surface of the silicon oxide insulation layer, this layer 20 is patterned and etched, forming bond pad 20 and interconnect points (not shown in Figs. 4-6) over the surface of the first layer 41 of metal
- a silicon dioxide insulation layer 40 is formed over the first metallic layer 41, including the surface of the created bond pad 20 and interconnect points
- a third metallic layer 30 is formed over the surface of the silicon dioxide insulation layer 40
- a photoresist mask (not shown in Figs. 4-6) is formed over the third metallic layer 30, having a covering over the planned pixel locations of the liquid-crystal-on-silicon display device

- the third metallic layer 30 that is not covered by the photoresist mask is removed
- the photoresist mask is removed to provided such that each pixel 30 retains the metallic layer 30, which acts as a mirror reflector for light incident upon the liquid-crystal-on-silicon display device
- an optical interference layer 60, comprising silicon oxide/silicon nitride/silicon oxide/silicon nitride, is deposited over the patterned third metallic layer 30 and the silicon oxide layer 40, and
- openings are created through the optical interference layer 60 and the silicon-oxide insulation layer 40, these openings expose the surfaces of bond pad 20 and interconnections (not shown) created on the surface of the first layer 41 of metal.

IN THE CLAIMS

1. (Amended) A method of forming insulating material alignment posts associated with active device structures comprising:

providing a silicon semiconductor wafer having patterned said active device therein and thereon; and

forming said insulating material alignment posts in a pattern over said pattern of active device structures, said

Serial number 09/262,000 insulating material alignment posts comprising an optical interference multilayer stack in addition to comprising an optical interference layer.

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8. (Amended) A method of forming a device structure that combines insulating materials for alignments posts and optical interference layers associated with an active device structure in a silicon body comprising:

providing a silicon [semiconductor] wafer having a pattern of active device structures therein and thereon;

forming a first metallic layer [there] over the surface of said wafer;

[forming a silicon-oxide insulation layer over the said first metallic layer;]

forming a second metallic layer over the said silicon oxide, which is used both for connections and for bonding pads;

forming a silicon dioxide insulation over the said second metal layer;

forming a third metallic layer [thereover] over the surface of said layer of silicon dioxide;

forming a photoresist mask over the said third metallic layer having a covering over the planned pixel locations of the said liquid-crystal-on-silicon display device;

removing the said third metallic layer not covered by the said photoresist mask;

removing the said photoresist mask to provide that each said pixel retains said metallic layer, which shall act as a mirror reflector for the light incident upon said liquid-crystal-on-silicon display device; and

depositing [the said] optical interference layers of silicon oxide/silicon nitride/silicon oxide/silicon nitride over said third metallic layer and said silicon [oxide] dioxide layer.

- 22. (Amended) The method of claim 17 for [of] etch-back removal of said silicon nitride, except that silicon nitride deposited in the said post cavities.
- 33. Please cancel claim 33.
- 34. Please cancel claim 34.
- 35. Please cancel claim 35.
- 36. Please cancel claim 36.